REMARKS/ARGUMENTS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-10 and 21-25 are pending in this case. Claims 1, 6, and 21 are amended herein.

The Examiner rejected claims 21-25 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claim 21 is amended to overcome the rejection by removing the term PMD.

The Examiner rejected claims 21-25 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter with applicant regards as the invention. Claim 21 is amended to overcome the rejection by removing the term PMD.

The Examiner rejected claims 1-3, 5 and 21-25 under 35 U.S.C. § 102(e) as being anticipated by Oda, of record, for the reasons given in the previous actions, hereby incorporated by reference.

Amended claim 1 requires, in an integrated circuit, a semiconductor device comprising a transistor gate, a contact layer, and a dielectric layer disposed inwardly from the contact layer and outwardly from the semiconductor device. The dielectric layer comprises an at least substantially porous dielectric material doped with at least one dopant. Furthermore, the dielectric layer laterally surrounds the transistor gate.

Applicant respectfully submits that amended claim 1 is unanticipated by Oda as there is no disclosure or suggestion in Oda of a dielectric layer comprising an at least substantially porous dielectric mat rial doped with at least one dopant, wherein the

dielectric lay r laterally surrounds the transistor gate and is disposed inwardly from the contact layer and outwardly from the semiconductor device. Oda teaches a porous dielectric layer doped with fluorine. However, the porous dielectric layer 10 is used above the first metal interconnect layer 7, not inwardly of the first metal interconnect layer 7 and does not laterally surround a transistor gate as required by the claim. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Oda.

Applicant respectfully submits that amended claim 21 is unanticipated by Oda as there is no disclosure or suggestion in Oda of a dielectric between a lowermost metal interconnect layer and the semiconductor substrate, the dielectric comprising an at least substantially porous dielectric material doped with at least one dopant and a contact extending through the dielectric from the lowermost interconnect layer, wherein the contact is laterally separated from the transistor gate by the dielectric. The porous dielectric of Oda is located outwardly of the first metal interconnect layer and vertically separated from where a transistor gate would be formed. Therefore, it cannot laterally separate a contact from a transistor gate, as required by the claim. Accordingly, Applicant respectfully submits that claim 21 and the claims dependent thereon are unanticipated by Oda.

The Examiner rejected claims 4 and 6-10 under 35 U.S.C. § 103(a) as being unpatentable over Oda, and further in view of Tseng, both of record, for the reasons given in the previous actions, hereby incorporated by reference.

Applicant respectfully submits that claim 4 is patentable over Oda in view of Tseng for the same reasons discussed above relative to claim 1 from which claim 4 depends. Tseng is added to teach a FET as a semiconductor device structure.

Applicant respectfully submits that amended claim 6 is patentable over Oda in view of Tseng as there is no disclosure or suggestion in the references of a substantially porous, doped dielectric layer dispos d inwardly from the contact layer,

outwardly from the semiconductor substrate, and laterally from the transistor gate, wherein a portion of a contact layer extends through the dielectric layer and is laterally separated from the transistor gate by the dielectric layer. Oda teaches a doped porous dielectric layer 10 located outwardly from the first metal interconnect layer. There is no disclosure or suggestion of a doped, porous dielectric disposed laterally from a transistor date. While Oda does teach a via 15 extending through the porous dielectric 10, via 15 is not a contact that is laterally separated from the gate by the doped, porous dielectric. Accordingly, Applicant respectfully submits that claim 6 and the claims dependent thereon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-10 and 21-25. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,
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